

Hyperband television tuner

TUN14474

FEATURES

- VHF/Hyperband / UHF tuner
- Systems CCIR: B/G, H
- Digitally controlled (PLL) tuning via I²C-bus
- Off-air channels, S-cable channels and Hyperband
- World standardized mechanical dimensions and world standard pinning
- Compact size
- Automatic bandswitching (UTS), independent of software
- Comply to "CENELEC EN55020" and "EN55013"

DESCRIPTION

TUN14474 belong to the family of tuner, which are designed to meet a wide range of applications. It is a combined VHF/Hyperband/ UHF tuner suitable for CCIR systems B/G and H. The IF output can drive a SAW filter directly and has capability to drive a asymmetrical load. The tuners comply with the requirements of radiation, signal handling capability and immunity conforming with:

- CISPR 13 (1990), including amendment 1 (1992) and amendment 2 (1993)
- European standards CENELEC EN55013, EN55020

ORDERING INFORMATION

TYPE	SYSTEM	DESCRIPTION
TUN14474	CCIR	asymmetrical IF output; IEC connector (14.5 mm), I ² C status byte

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INTERMEDIATE FREQUENCIES

SIGNAL	FREQUENCY (MHz)	
	SYSTEM	B/G, H
Picture carrier	38.90	
Colour	34.47	
Sound	33.40	

Note

1. The oscillator frequency is above the input signal frequency.

CHANNEL COVERAGE

Type	BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
		CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
TUN14474	Low band	E2 to Z	48.25 to 83.25 ⁽¹⁾	S01 to S06	69.25 to 140.25
	Mid band	E5 to E12	175.25 to 224.25	S07 to S36	147.25 to 423.25
	High band	E21 to E69	471.25 to 855.25 ⁽²⁾	S37 to S41	431.25 to 463.25

Notes

- 1. Enough margin is available to tune down to 45.25 MHz.
- 2. Enough margin is available to tune up to 863.25 MHz.

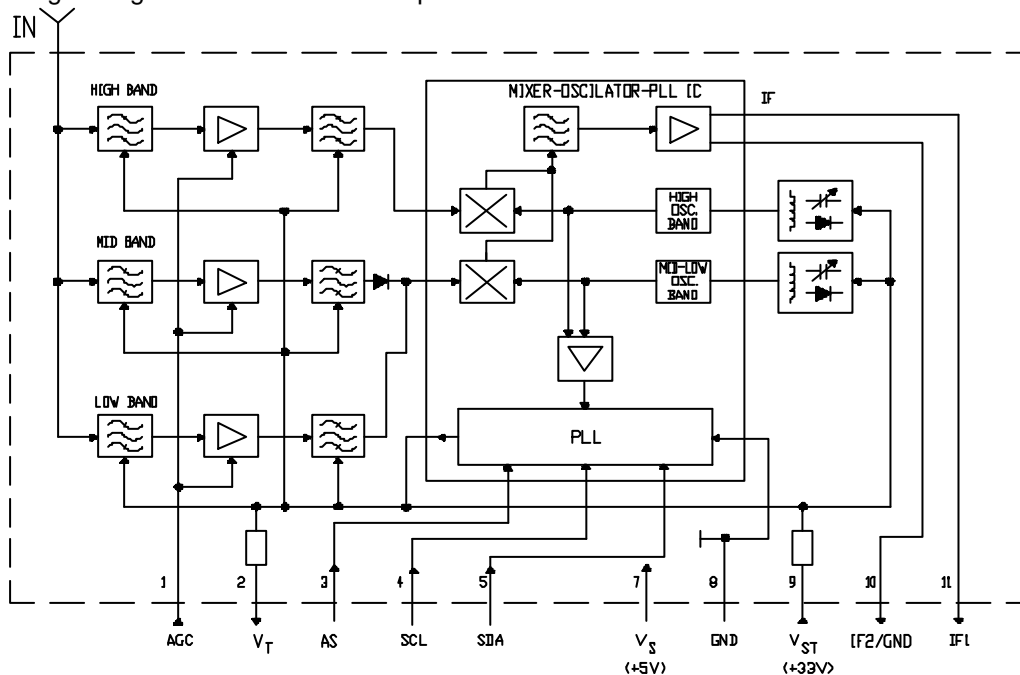


Fig.1 Electrical block diagram

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PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	gain control voltage
V _T	2	tuning voltage
AS	3	I ² C-bus address select
SCL	4	I ² C-bus serial clock
SDA	5	I ² C-bus serial data
n.c.	6	not connected
V _S	7	PLL supply voltage +5 V
M	8	Ground (mode selection)
V _{ST}	9	tuning supply voltage +33 V
IF2	10	ground
IF1	11	asymmetrical IF output
GND	MT1, MT2	mounting tags (ground)
IN		aerial input connector IEC (14.5 mm)

LIMITING VALUES

Environmental conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Non-operational conditions				
T _{amb}	ambient temperature	-40	+60	°C
RH	relative humidity	-	100	%
Operational conditions				
T _{amb}	ambient temperature	-15	+60	°C
RH	relative humidity	-	93	%

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Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions

SYMBOL	PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
V_S	supply voltage	7	4.75	5.00	5.5	V
I_S	supply current		-	-	130	mA
V_{ST}	supply voltage	9	30	33	35	V
I_{ST}	supply current		-	-	1.7	mA
V_{AGC}	AGC input voltage	1	-	4.0	4.5	V
ΔV_{AGC}	AGC input voltage range		0.3	-	4.0	V
I_{AGC}	AGC input current		-	-	20	μ A
V_{AS}	address select input voltage	3	-	-	5.5	V
V_{SCL}	serial clock input voltage	4	-	-	5.5	V
V_{SDA}	serial data input voltage	5	-	-	5.5	V
I_{SDA}	serial data input current		-1	-	5	mA

ELECTRICAL DATA

Conditional data

Unless otherwise specified, all electrical values for Chapter "Electrical data" apply at the following conditions and the electrical performance is related both to systems B, G and H.

A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T_{amb}	ambient temperature	25 +/- 5	$^{\circ}$ C
RH	relative humidity	60 +/- 15	%
V_S	supply voltage	5.0 +/- 0.1	V
V_{AGC}	AGC input voltage	4.0 +/- 0.1	V
V_{ST}	tuning supply voltage	33 +/- 0.5	V
t_{pr}	pre-heating time (+5 V at pin 7)	10	minute
$Z_{S(AE)}$	aerial source impedance (unbalanced)	75	Ω

Aerial input characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VSWR	Reflection coefficient	referred to 75 Ω impedance	-	2	4	
V_{ant}	antenna connection disturbance voltage	< 1.75 GHz; comply to "EN55013 section 3.3"	-	-	46	dB μ V

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General characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT				
f_p	frequency range:									
	low band		48.25	-	140.25	MHz				
	mid band		147.25	-	423.25	MHz				
	high band		431.25	-	855.25	MHz				
Y	RF-curves, tilt	The IF output is loaded with a test circuit according diagram fig.2	-	2.5	4.0	dB				
G_v	voltage gain:	The IF output is loaded with a test circuit according diagram fig.2	36	45	52	dB				
	all channels gain taper						-	-	7	dB
F	noise:	The IF output is loaded with a test circuit according diagram fig.2	-	7.0	9	dB				
	low band						-	6.0	9	dB
	mid band						-	5.0	8	dB
	high band									
ΔV_{AGC}	AGC input voltage range:	The IF output is loaded with a test circuit according diagram fig.2	45	60	-	dB				
	low and mid band						40	50	-	dB
	high band									
α_i	image rejection:		66	70	-	dB				
	low band						60	69	-	dB
	mid band						50	60	-	dB
	high band									
α_{IF}	IF rejection (picture):		55	68	-	dB				
	channel E2						65	71	-	dB
	low, mid and high bands									
V_{ESD}	electrostatic discharge (ESD):	note 1	2	-	-	kV				
	protection on pins 1 to 5 and 6 to 11						8	-	-	kV
	protection on antenna socket									
	oscillator characteristics:		-	-	note 2	kHz				
	oscillator tuning resolution						-	-	150	msec
	lock-in time									

Notes

1. The tuner meets specifications IEC 1000-4-2 level 1 for pins and level 4 for antenna socket.
2. Resolution 31.25 kHz, 50.00 kHz, 62.5 kHz or 166.7 kHz (see Table "Ratio select bits").

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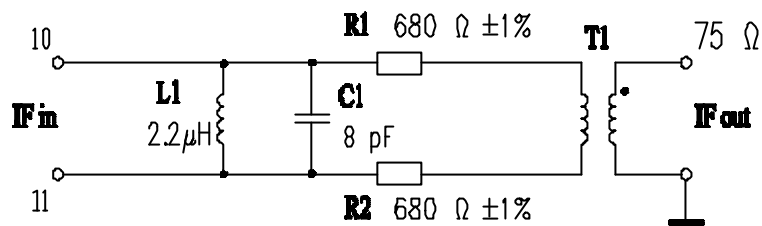
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Visibility test

The tuners meet the requirements of the European norm "EN55020", when measured in an adequate television receiver.

Radiation

The tuners meet the requirements of the European norm "EN55013" and "CISPR13" (1990), when measured in an adequate television receiver.



Dummy Attenuation = 22.6 dB

T1 – RF Transformer.
 W – Ratio = 1:4 (IF – IN = 4 / IF – OUT = 1).
 Type: MCL T4-1 or equivalent.

Fig. 2 Test circuit

Recommended adjustment of Tuner AGC in TV chassis:

- Channel: E21 (471.25 MHz PC-frequency)
- Input level: 70 dB μ V/75 Ω
- IF output level: 105 dB μ V
- Gain reduction: 10 dB
- AGC-Voltage: 2.6 V +/-0.2V

AGC characteristics shown on Fig. 6

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APPLICATION INFORMATION

WRITE mode

BYTE	BITS									
	7 MSB	6	5	4	3	2	1	0 LSB	A ⁽²⁾	Mod e ⁽¹⁾
Address byte	1	1	0	0	0	MA1	MA0	0	A	
Program divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A	
Program divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A	
Control byte	1	CP	x	x	x	RSA	RSB	OS	A	1
Control byte	1	x	x	x	x	x	x	x	A	2
Control byte	1	CP	T1	T0	FP	RSA	RSB	OS	A	4
Bandswitch byte	x	x	x	x	x	x	x	x	A	1, 2
Bandswitch byte	x	x	x	x	x	PHIGH	PLOW	PMID	A	4

Notes

1. See mode selection.
2. A = Acknowledge.
3. X = don't care.

Address selection

V_s = 5 V (PLL supply voltage).

MA1	MA0	VOLTAGE AT PIN 3
0	0	(0...0.1)*V _s
0	1	Open circuit
1	0	(0.4...0.6)*V _s
1	1	(0.9...1)*V _s

Programmable divider settings (bytes 1 and 2)

Divider ratio:

$$N = R \times \{ f_{RF,pc} + f_{IF,pc} \}, \quad R = \text{Step size}$$

$$N = (16384 \times n14) + (8192 \times n13) + (4096 \times n12) + (2048 \times n11) + (1024 \times n10) + (512 \times n9) + (256 \times n8) + (128 \times n7) + (64 \times n6) + (32 \times n5) + (16 \times n4) + (8 \times n3) + (4 \times n2) + (2 \times n1) + n0$$

Charge pump settings (bit CP)

CP can be set to either 0 (low current = 50 μA) or 1 (high current = 220 μA).

Charge pump settings:

CP = 1, for fast tuning

CP = 0, for moderate speed tuning with slightly better residual oscillator FM.

Unnecessary charge pump action will result in very low tuning voltage (V_T=0V) which may drive the oscillator to extreme conditions.

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Reference divider ratio

RSA	RSB	REFERENCE DIVIDER	f _{ref} (kHz)
X Modes 1 to 3	0	80	50
0 Mode 4	0	80	50
1 Mode 4	0	24	166.7
0	1	128	31.25
1	1	64	62.5

Mode selection

Mode	Voltage at pin 8	Description
1	(0...0.1)*Vs	Normal operation, UTS (automatic bandswitching) enabled, bandswitch bits are disabled, Control byte is enabled, reference divider ratios 128, 80 and 64 are addressable, automatic I/5I switch is disabled
2	open circuit	UTS function enabled, bandswitch bits are disabled, Control byte is disabled, reference divider ratio is 64, automatic I/5I switch is enabled ¹⁾
3	(0.4...0.6)*Vs	Not in use
4	(0.9...1)*Vs	UTS function disabled, bandswitch bits are enabled, Control byte is enabled, reference divider ratios 128, 80 and 64 are addressable, automatic I/5I switch is disabled

1). Whenever lock of the PLL is lost, CP is switched to "5I". It returns to "I" if the PLL is locked again.

Band switching in Mode 4

BITS								BAND
7 MSB	6	5	4	3	2	1	0 LSB	
X	X	X	X	X	0	1	0	Low band
X	X	X	X	X	0	0	1	Mid band
X	X	X	X	X	1	0	0	High band

READ mode

BYTE	BITS								
	7 MSB	6	5	4	3	2	1	0 LSB	A ⁽¹⁾
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	POR ⁽²⁾	FL ⁽³⁾	x	X	x	x	x	x	A

Notes

1. A = Acknowledge.
2. POR = Power On Reset flag (POR=1 at power on).
3. FL = In-lock flag (FL=1 at loop is phase-locked).

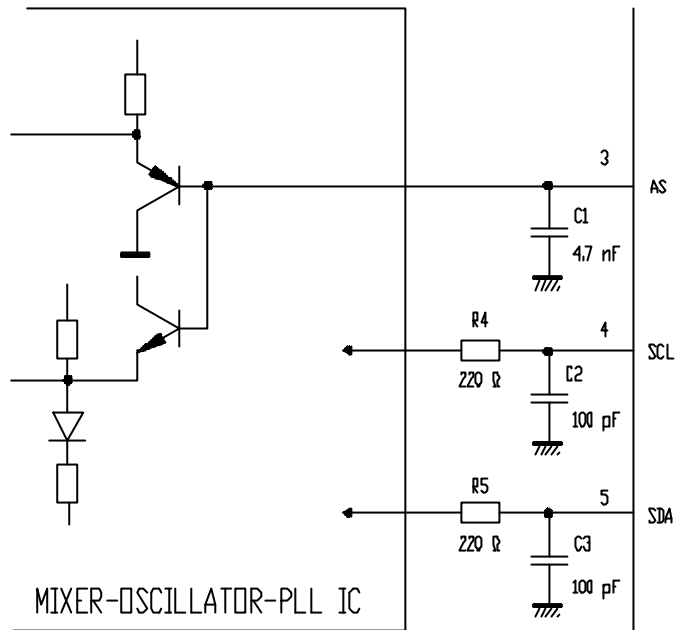


Fig.3 I²C-bus load.

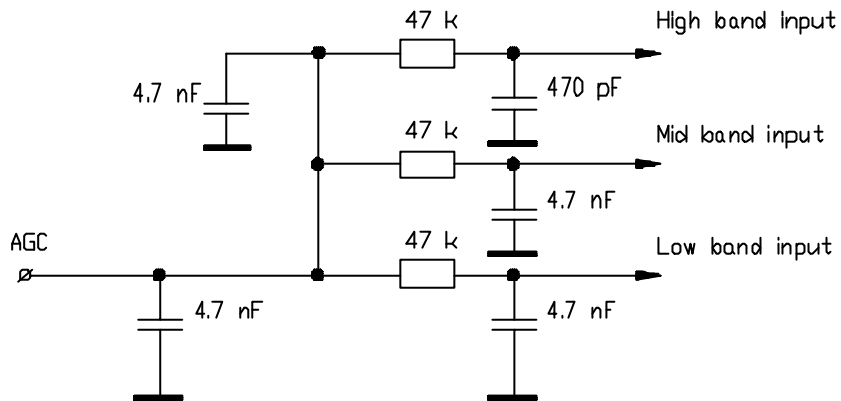


Fig.4 Internal AGC circuit.

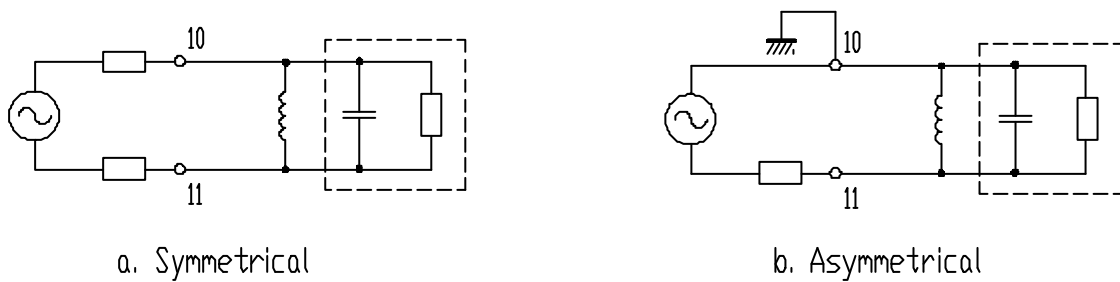


Fig.5 IF loading using SAW filters

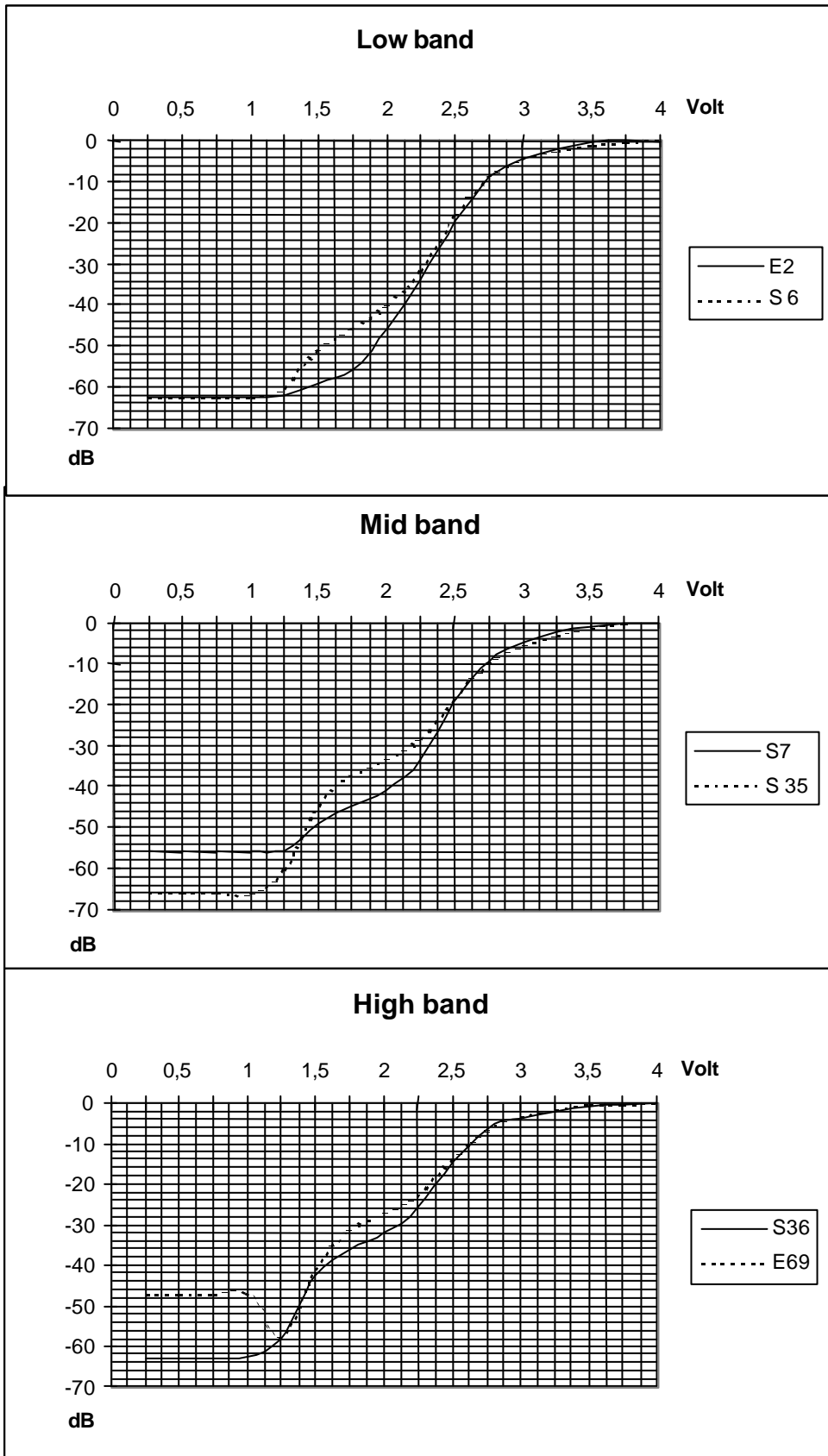


Fig.6 AGC characteristics.

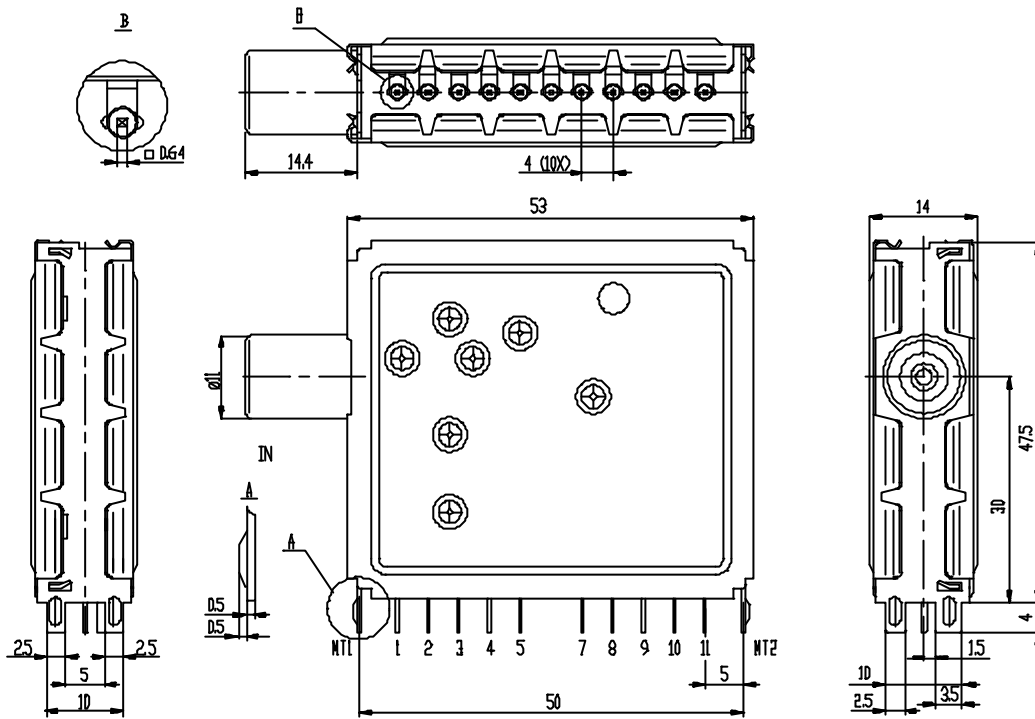


Fig.7 Mechanical outline

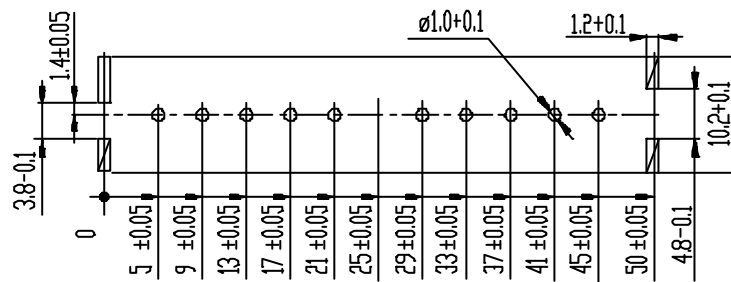


Fig.8 Punching pattern seen from solder side

Aerial connections

Standard IEC socket female 75 Ω.